

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1-20. (canceled)

21. (new) A method of manufacturing a semiconductor device, comprising:

forming a fin;

forming a gate structure over a portion of the fin;

forming a dielectric layer adjacent the gate structure;

etching the gate structure to form a gate recess; and

depositing a metal in the gate recess.

22. (new) The method of claim 21, further comprising:

removing the dielectric layer.

23. (new) The method of claim 21, further comprising:

depositing a cap layer on a semiconducting layer, and wherein the forming a fin includes:

etching the cap layer and the semiconducting layer to define the fin and a cap over the fin.

24. (new) The method of claim 21, wherein the forming a gate structure comprises:

depositing a gate material over the fin, and  
planarizing the deposited gate material.

25. The method of claim 24, wherein the depositing a gate material comprises:  
depositing silicon over the fin.

26. (new) The method of claim 24, wherein the forming a gate structure further comprises:

depositing an antireflective coating on the planarized gate material,  
depositing a photoresist layer over the antireflective coating, and  
 patterning the photoresist layer to define the gate structure.

27. (new) The method of claim 21, wherein the forming a dielectric layer comprises:  
depositing an oxide material over the gate structure, and  
polishing the oxide material until a top surface of the gate structure is exposed and  
a remaining portion of the oxide material is substantially coplanar with the exposed top  
surface of the gate structure, wherein the remaining oxide material acts as a mask to  
prevent etching of underlying layers.

28. (new) The method of claim 21, further comprising:  
depositing a dielectric material over a portion of the fin in a channel region of the semiconductor device prior to depositing the metal.
29. (new) The method of claim 21, further comprising:  
polishing the metal to define a metal gate.
30. (new) The method of claim 29, wherein the metal comprises at least one of tantalum and titanium.
31. (new) A method of manufacturing a semiconductor device, comprising:  
forming a fin on an insulator;  
forming a gate structure, the gate structure extending over a channel portion of the fin;  
forming a sacrificial layer adjacent the gate structure;  
removing the gate structure to define a gate recess; and  
forming a metal gate in the gate recess.
32. (new) The method of claim 31, further comprising:  
removing the sacrificial layer.
33. (new) The method of claim 31, further comprising:  
forming a dielectric layer on a portion of the fin before forming the metal gate.

34. (new) The method of claim 33, wherein the dielectric layer has a dielectric constant greater than about 3.9.

35. (new) The method of claim 31, wherein the forming the sacrificial layer comprises:

depositing an oxide layer over the gate structure and the fin, and  
polishing the oxide layer until a top surface of the gate structure is exposed.

36. (new) The method of claim 31, wherein the forming a metal gate comprises:  
depositing a metal in the gate recess, and  
planarizing the metal to define the metal gate.

37. (new) A semiconductor device, comprising:  
a substrate;  
an insulating layer formed on the substrate;  
a conductive fin formed on the insulating layer, the conductive fin including a plurality of side surfaces and a top surface;  
a source region formed on the insulating layer adjacent a first end of the conductive fin;  
a drain region formed on the insulating layer adjacent a second end of the conductive fin; and  
a metal gate formed on the insulating layer adjacent the conductive fin in a channel region of the semiconductor device.

38. (new) The semiconductor device of claim 37, further comprising:  
a dielectric layer formed on the top surface and side surfaces of the conductive fin  
in the channel region of the semiconductor device.
39. (new) The semiconductor device of claim 38, wherein the dielectric layer has  
a dielectric constant greater than about 3.9.
40. (new) The semiconductor device of claim 37, wherein the metal gate  
comprises at least one of titanium and tantalum.